FIG._1A
(PRIOR ART)

FIG._1B
(PRIOR ART)

SOURCE 10

DESTINATION 30

ROUTER 20

ROUTER 20

ROUTER 20

DESTINATION 30

DESTINATION 30

FIG._2A

INPUT SECTION 150-0

INPUT SECTION 150-1

INPUT SECTION 150-2

INPUT SECTION 150-3

A_1 100

150-0
150-1
150-2
150-3

MEMORY 104

MEMORY BANK 0
MEMORY BANK 1
MEMORY BANK 2
MEMORY BANK 3

105

MEMORY SECTIONS OF MULTI FUNCTION PORTS

KEY

CONTROLLER 106

RLE 110

109

NOTIFICATION

A_2 102

OUTPUT SECTION 150-0

OUTPUT SECTION 150-1

OUTPUT SECTION 150-2

OUTPUT SECTION 150-3

20

FIG._2B

INPUT
SWITCH
100

305
304
306
150
280
316
318

REQUEST
PROCESSOR

HEAD
AND
TAIL
QUEUE
BUFFER

308

SWITCH
102

310

MEMORY

312

BUFFER

314

LINE

300

LINE
INPUT

302

DATA
HANDLER

270

INPUT
SWITCH
100

304

105

GLOBAL
DATA
AREA
(MEMORY
BANK)

NOTIFICATION
AREA

319

290

FIG._3A

FIG._3B

	356	358	360	
350	TYPE	STREAM	PACKET HEADER	
366	OUTPUT PORT ID	ADDRESS 368		352
354	CELL DATA			

FIG._3C

FIG._4

CONTROLLER — 106

512

100

505

OUTPUT
PROCESSOR

ROUND ROBIN
DATA HANDLER — 500

501-0

INDIRECT
CELL
MEMORY — 520

504-0 — 502-0

501-1

502-1

504-1

514

510

KEY
READING
ENGINE

INDIRECT
CELL
PROCESSOR

501-2

504-2 — 502-2

516

KEY
BUFFER

508

501-7

515

LINKING
ENGINE

RESERVA-
TION
TABLE

504-7 — 502-7

READ CONTROLLER — 517

506-0   506-1   506-2   506-7
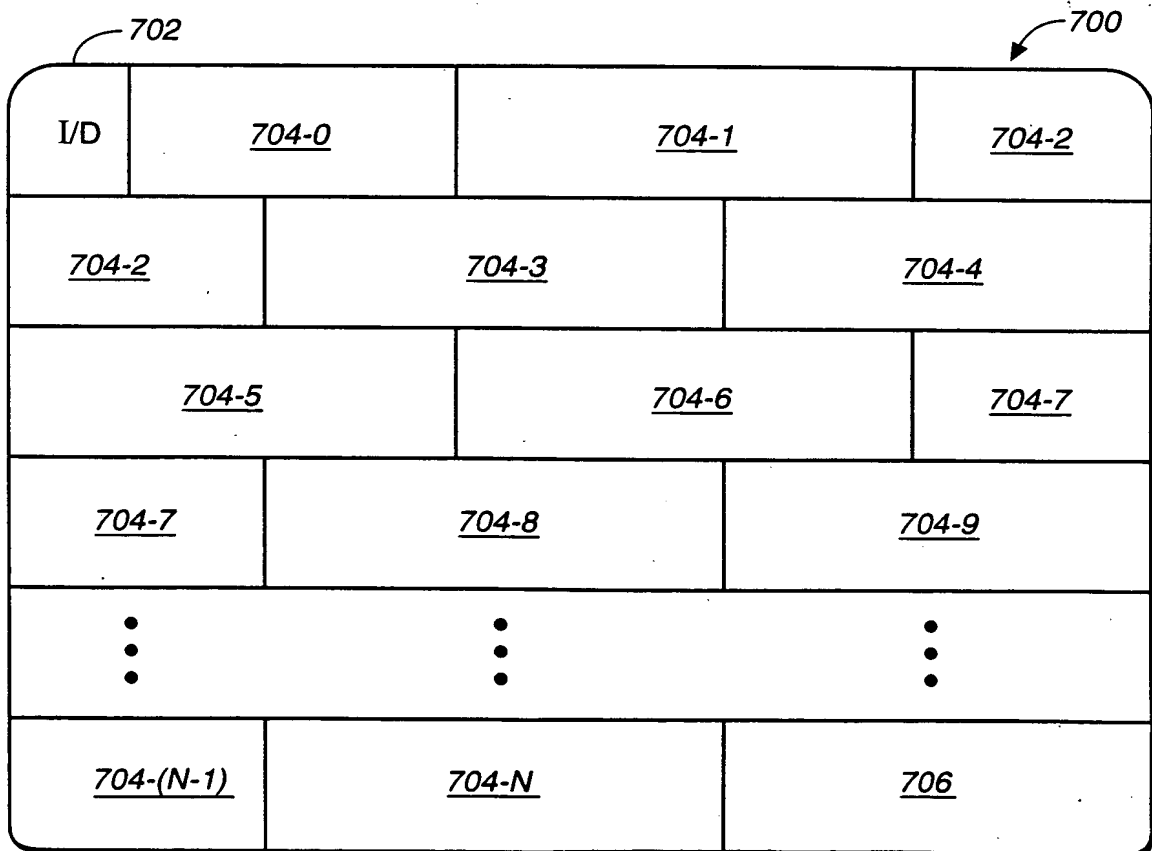
READ REQUEST INPUTS
FROM MULTI-FUNCTION
MULTIPORTS 150

FIG._5A

FIG._5B

I	KEY	FULL ADDRESS	OFFSET 0	OFFSET 1	OFFSET 2	OFFSET 3

600
608 602 604   606   606   606   606

FIG._6

I/D	704-0	704-1	704-2
704-2	704-3		704-4
704-5	704-6		704-7
704-7	704-8		704-9
⋮	⋮		⋮
704-(N-1)	704-N		706

702   700

FIG._7

FIG._8

M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7

M_0	M_1	M_2	M_3	M_4	M_5	M_6	M_7	
B_7	B_0	B_1	B_2	B_3	B_4	B_5	B_6	902
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_0	902
B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	902
B_7	B_0	(B_1)	B_2	(B_3)	B_4	B_5	B_6	902
B_6	(B_7)	B_0	B_1	B_2	B_3	B_4	B_5	902
B_5	B_6	B_7	B_0	B_1	(B_2)	B_3	B_4	902
(B_4)	(B_5)	B_6	B_7	B_0	B_1	B_2	B_3	902
B_3	B_4	B_5	(B_6)	B_7	B_0	B_1	B_2	902
B_2	(B_3)	B_4	B_5	B_6	B_7	B_0	B_1	902
B_1	B_2	(B_3)	B_4	(B_5)	B_6	(B_7)	B_0	902
B_0	(B_1)	B_2	(B_3)	B_4	(B_5)	(B_6)	(B_7)	902

906

904

908

508

900-1   900-2   900-4   900-6

900-1   900-3   900-5   900-7

FIG._9

```
                ┌─────────────────┐
                │  RECEIVE READ   │      1000
                │    REQUEST      │
                └─────────────────┘
                         │
                         ▼
                ┌─────────────────┐
                │   DECODE READ   │      1002
        ┌──────▶│   REQUEST TO    │
        │       │ DETERMINE COLUMN│
        │       │    TO SEARCH    │
        │       └─────────────────┘
        │                │
        │                ▼
        │       ┌─────────────────┐
        │       │ SEARCH FOR FIRST│      1004
        │       │   PLACE HOLDER  │
        │       │    AVAILABLE    │
        │       └─────────────────┘
        │                │
        │                ▼
        │       ┌─────────────────┐
        │       │    TRANSFORM    │      1006
        │       │ PLACE HOLDER BY │
        │       │ STORING ADDRESS │
        │       └─────────────────┘
        │                │
        │                ▼
        │       ┌─────────────────┐
        │       │   LOAD NEXT     │      1008
        │       │  READ REQUEST   │
        │       └─────────────────┘
        │                │
        └────────────────┘
```

FIG._10

FIG._11A

304-0	MEMORY BANK M_0	105	316-0
304-1	MEMORY BANK M_1	105	316-1
304-2	MEMORY BANK M_2	105	316-2

104

MEMORY BANK M_0 105

MEMORY BANK M_1 105

MEMORY BANK M_2 105

•
•
•

MEMORY BANK M_7 105

319

NOTIFICATION QUEUES

FIG._11B

PBN – SLOT # 0

FIG._11C

104

105 105 105 105

M_0 M_1 M_2 • • • M_7

1260

T_3 B_0 B_1 B_2 B_7

T_4 B_1 B_2 B_3 B_0

100

INPUT SWITCH

1250

T_1 M_0 M_1 M_2 M_7

T_2 M_1 M_2 M_3 M_0

150-0 B_0

150-1 B_1

150-2 B_2

• • •

150-7 B_7

FIG._12

*FIG._13*A

MASK	NEXT HOP INDEX POINTER		PACKET LENGTH	
FULL ADDRESS		OFFSET 0	OFFSET 1	OFFSET 2	OFFSET 3

1402 *1404* *1410* *1400*
1406 *1408* *1408* *1408* *1408*

FIG._14

START
NODE — 2300

ROUTE
NODE — 2306

INTERNAL
NODE — 2302

INTERNAL
NODE — 2302

ROUTE
NODE — 2306

ROUTE
NODE — 306

INTERNAL
NODE
WITH
ATTACHED
ROUTE — 304

ROUTE
NODE — 306

FIGURE 13 B

2400 — BIT TO TEST (00)
2402 — LEFT CHILD Pointer
2403 — LEFT CENTER PTR
2404 — Right CHILD PTR
2405 — Right CENTER PTR
2406 — ATTACHED Route

13 D

BIT TO TEST	2400
LEFT CHILD POINTER	2402
RIGHT CHILD POINTER	2404
ATTACHED ROUTE	2406
- - - - - -	

FIGURE 13C

STUB NODE

2402 —	LEFT CHILD POINTER
2404 —	RIGHT CHILD POINTER
2406 —	ATTACHED ROUTE
	- - - - - -

FIGURE 13E

| ATTACHED ROUTE | 2406 |
| - - - - - - | |

FIGURE 13F

BIT TO TEST	2400
LEFT CHILD POINTER	2402
RIGHT CHILD POINTER	2404

FIGURE 13G

CREATE START NODE — 2500

ASSIGN ATTACHED ROUTE TO START NODE — 2502

ASSIGN LEFT AND RIGHT CHILD POINTERS A "O" VALUE — 2504

STORE START NODE IN MEMORY — 2506

ANY OTHER KEY? — 2508
YES
NO

3 → END — 2510

LOAD NEXT KEY — 2512

ADD KEY AS ROUTE NODE — 2514

ASSIGN A ROUTE TO ROUTE NODE BASED ON DESTINATION — 2516

STORE ROUTE NODE IN MEMORY — 2518

UPDATE POINTER IN START NODE — 2520

ANY OTHER KEYS? — 2522
YES
NO

2523 — a

LOAD NEXT KEY

PERFORM PREFIX SEARCH — 2524

LOCATE "END" ROUTE — 2526

COMPARE "END" ROUTE AND KEY — 2528

ARE THERE ANY DISSIMILAR BITS? — 2529
YES → A
NO → B

FIGURE 13H

A

CREATE NEW ROUTE
NODE & STORE IN
MEMORY — 2530

CREATE NEW
INTERNAL
NODE — 2532

ASSIGN BIT TO
TEST VALUE EQUAL
TO BIT_{DIS} — 2534

ASSIGN ONE CHILD
POINTER ADDRESS
OF NEW ROUTE NODE — 2536

TRAVERSE TREE
BACKWARDS
TO LOCATE PARENT
NODE — 2538

INSERT NEW NODE
BETWEEN PARENT AND
GRAND-CHILD NODE — 2540

UPDATE POINTER
IN PARENT
NODE — 2542

1

FIGURE 13I

B

COMPARE LENGTH OF KEY WITH "END" ROUTE — 2545

IS KEY LONGER THAN "END" ROUTE? — 2546

YES — B1

NO

IS THE KEY SHORTER? — 2547

YES — B2

NO

B3

FIGURE 13J

(B1)

CREATE NEW
ROUTE NODE &
STORE IN MEMORY → 2550

IS 'END'
NODE A ROUTE
NODE ? → 2552

NO

YES

2554 → ASSIGN Child Pointer
IN INTERNAL NODE
THE ADDRESS of NEW
ROUTE

CREATE NEW
INTERNAL
NODE → 2556

ASSIGN BIT TO TEST
FOR NEW INTERNAL
NODE TO BE LAST BIT
IN 'END' ROUTE → 2558

ASSIGN ONE Child
POINTER THE ADDRESS
of NEW ROUTE NODE → 2560

2562 → UPDATE ADDRESS
of POINTER IN
PARENT NODE

(1)

FIGURE   13 K

B2

LOCATE PARENT NODE ~570

IS BIT TO TEST LESS THAN INDEX OF KEY? ~571

Yes

No

INSERT NEW INTERNAL NODE BELOW PARENT ~572

UPDATE ATTACHED ROUTE IN PARENT NODE ~590

ASSIGN BIT TO TEST THE VALUE OF THE INDEX OF THE KEY ~574

ASSIGN ONE POINTER THE STARTING ADDRESS OF THE GRAND-CHILD NODE ~576

ASSIGN OTHER POINTER A ZERO VALUE ~578

UPDATE POINTER IN PARENT NODE ~580

1

FIGURE 13L

B3

UPDATE "END" ROUTE — 2592

1

FIGURE 13M

1

ANY MORE KEYS? — 2598

No → 3

YES

2

FIGURE 13N

DETERMINE KEY TYPE ● 2600

LOAD START NODE 2602

DETERMINE BIT VALUE of BIT IN KEY INDICATED BY BIT TO TEST INDICATOR 2604

DOES POINTER POINT TO A CHILD NODE? 2606
No → C
Yes ↓

DOES START NODE HAVE AN ATTACHED ROUTE 2608
No → G
Yes ↓

F → STORE BIT TO TEST INDICATOR AND ROUTE ADDRESS ON STACK 2610

G → LOAD NEXT NODE 2612

IS NODE A ROUTE NODE? 2614 ●
Yes → C
No ↓

DETERMINE VALUE OF BIT IN KEY INDICATED BY BIT TO TEST INDICATOR 2616

DOES POINTER INDICATE A CHILD NODE 2618
No → C
Yes ↓

DOES NODE HAVE AN ATTACHED ROUTE? 2620
Yes → F
No ↓

G

FIGURE 13P

C

DETERMINE FIRST
DISSIMILAR BIT
IN KEY — 2630

ANY
DISSIMILAR
BITS! — 2632

YES → D

NO

E

D

TRAVERSE TRIE
BACKWARDS AND
LOCATE BEST MATCH
NODE — 2640

E

E

LOAD BEST MATCH
ROUTE — 2650

TRANSFER
ROUTE TO
OUTPUT SWITCH — 2652

END

FIGURE   13Q

FIGURE 13 R

2704 2706 2708 2710

| r | R | POINTER FIELD | Btt | ← 2700 |
| r | R | POINTER FIELD | Btt | ← 2702 |

FIGURE 13 S

2710 2704 2706 2708

| r | R | POINTER FIELD | Btt | ← 2700 |
| r | R | POINTER FIELD | Btt | ← 2702 |

RESULT 2722 ← 2720

| PREFIX 2722 | INDEX 2724 |
| STATISTICS 2728 | QOS 2730 |

FIGURE 13 T

← 2710

RESULT 2722

| PREFIX 2722 | INDEX 2724 |
| STATISTICS 2728 | QOS 2730 |

FIGURE 13.u

DETERMINE KEY TYPE 800

DETERMINE STARTING ADDRESS OF TRIE 802

IS BIT ZERO OF KEY A "0"? 804
TES →
NO ↓

INCREMENT ADDRESS 807

RETRIEVE RIGHT CHILD POINTER 808

RETRIEVE LEFT CHILD POINTER 806

DOES POINTER POINT TO A ROUTE NODE 810
NO →
YES ↓

RETRIEVE ROUTE 812

(4)

STORE POINTER ON STACK IF R=1 814

IS BIT TO TEST A "0"? 815
NO →
YES ↓

RETRIEVE LEFT CHILD 816

RETRIEVE RIGHT CHILD 818

DOES POINTER POINT TO A ROUTE? 820
YES
NO ↓

IS THE POINTER VALUE NULL? 822
NO →
YES ↓

DOES NODE HAVE AN ATTACHED ROUTE? 824
YES →
NO ↓

IS STACK EMPTY 825
NO →
YES → ERROR 826

RETRIEVE ROUTE FOR LAST STACK ENTRY 828

(4)

(4)

```
┌─────────────────────┐
│  DETERMINE          │  ⟍2830
│  FIRST DISSIMILAR   │
│  BIT                │
└─────────────────────┘
          │
          ▼
      ╱───────────╲          2832
     ╱  ANY DISSIMILAR ╲  ─── YES ──►  ┌──────────────────────┐
     ╲    BITS ?       ╱               │  TRAVERSE TREE       │ ⟍2840
      ╲───────────╱                    │  BACKWARDS TO        │
          │                            │  LOCATE BEST MATCH   │
          │ NO                         │  NODE                │
          ▼                            └──────────────────────┘
┌─────────────────────┐                          │
│  LOAD BEST          │ ⟍2850                    │
│  MATCH ROUTE        │ ◄────────────────────────┘
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│  TRANSFER           │ ⟍2852
│  ROUTE TO           │
│  OUTPUT SWITCH      │
└─────────────────────┘
```

FIGURE ~~8B~~ 13 ✓

FIG._15A

FIG._15B

1600 →	
1606 —	SOURCE ID
1608 —	ROUTE INFORMATION
	DATA FIELD

1602

1604

FIG._16

FIG._17A

FIG._17B

RECEIVE DATA PACKET — 1800

DIVIDE PACKET INTO FIXED LENGTH CELLS — 1802

EXTRACT KEY AND STORE IN KEY BUFFER — 1804

ROUTE CELLS TO MEMORY BANKS — 1806

STORE ADDRESS OF FIRST CELL AND OFFSETS — 1808

CREATE INDIRECT CELLS — 1810

TRANSFER ROUTE REQUEST TO CONTROLLER — 1814

1816 — LOOK UP DESTINATION AND GENERATE RESULT

1818 — TRANSFER RESULT TO OUTPUT SWITCH

1820 — GENERATE READ REQUEST AND TRANSFER TO INPUT SITE

1822 — ISSUE READ REQUEST TO MEMORY

1824 — WRITE CELL DATA AND OUTPUT PORT ID

1826 — COUPLE CELL DATA AND MEDIA HEADER AND STREAM DATA

FIG._18